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Description

[INCREASE PRODUCTIVITY AT WAFER TEST USING PROBE RETEST DATA ANALYSIS]

Background of Invention

[0001] Field of the Invention

[0002] The invention presents a method and system for wafer/probe testing integrated circuit devices after manufacture which optimizes the retest process.

[0003] Description of the Related Art

[0004] Every test facility deals with the problem of not having enough tools to handle the capacity on high volume products. The options to alleviate this issue are either to purchase more testers or to reduce test cycle time (increase productivity). Since a new tester costs millions and lead times are long, using probe data analysis to increase productivity is the most cost effective solution.

Summary of Invention

[0005] The invention presents a method and system for wafer/probe testing integrated circuit devices after manufacture. The invention begins by testing an initial group of devices (e.g., integrated circuit chips) to produce an initial failing group of devices that failed the testing. The devices in the initial failing group are identified by type of failure. Then, the invention retests the devices in the initial failing group to identify a retested passing group of devices that passed the retesting. Next, the invention analyzes the devices in the retested passing group which allows the invention to produce statistics regarding the likelihood that a failing device that failed the initial testing will pass the retesting according to the type of failure. Then, the invention evaluates these statistics to determine which types of failures have retest passing rates above a predetermined threshold. From this the invention produces a database comprising an optimized retest table listing the types of defects that are approved for retesting.

[0006] The invention can also identify types of devices having a predetermined reduced demand. For example, certain types of devices may no longer be in strong demand, and it may not be worth the cost to retest these types of devices. Therefore, in one option, the invention can add a

listing of item types having reduced demand to the database to prevent such reduced demand items from being retested.

[0007] Further, some types of defects may be known to be related to improper testing. One contributor to test failures is bad or marginal probe contact due to reasons that include poor test setup and marginal/defective probe hardware. In order to eliminate improper testing errors, the invention can add types of defects associated with testing errors to the types of defects approved for retesting.

[0008] Using the information in the optimized retest table database, the invention then tests additional groups of devices to produce additional failing groups of devices. The invention only retests devices that have one of the types of defects approved for retesting, and does not retest the types of devices for which there is reduced demand. This process optimizes the retesting of the devices by only retesting for defects that are above a predetermined retest passing rate.

[0009] The inventive system includes a tester (e.g., probe-type tester), a database, and a processor. The database includes an optimized retest table of the types of defects approved for retesting. Again, the types of defects ap-

proved for retesting are based upon previously acquired statistics of which types of failures have retest passing rates (after initially failing testing) above a predetermined threshold. In addition, defect types that result from improper testing are included in the types of defects approved for retesting. Once again, device types having reduced demand are not sometimes retested. The processor directs the tester to test groups of devices and retests only devices in the additional failing groups that have one of the types of defects approved for retesting, without testing device types that have reduced demand.

[0010] Thus, with the invention, the data collected at wafer test is analyzed to optimize limits and rules on retest without sacrificing yield. It is important to retest failed devices to avoid discarding properly functioning devices. By not retesting all failed devices and optimizing which devices are tested, substantial testing costs are saved.

[0011] These, and other, aspects and objects of the present invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following description, while indicating preferred embodiments of the present invention and nu-

merous specific details thereof, is given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the present invention without departing from the spirit thereof, and the invention includes all such modifications.

Brief Description of Drawings

[0012] The invention will be better understood from the following detailed description with reference to the drawings, in which:

[0013] Figure 1 is a flow diagram illustrating a preferred method of the invention;

[0014] Figure 2 is a table showing aspects of the invention;

[0015] Figure 3 is a table showing aspects of the invention;

[0016] Figure 4 is a table showing aspects of the invention;

[0017] Figure 5 is a table showing aspects of the invention;

[0018] Figure 6 is a table showing aspects of the invention;

[0019] Figure 7 is a table showing aspects of the invention;

[0020] Figure 8 is a table showing aspects of the invention;

[0021] Figure 9 is a table showing aspects of the invention;

[0022] Figure 10 is a table showing aspects of the invention;

[0023] Figure 11 is a system embodiment of the invention; and

[0024] Figure 12 is a schematic hardware diagram upon which the invention could operate.

DETAILED DESCRIPTION

[0025] The present invention and the various features and advantageous details thereof are explained more fully with reference to the nonlimiting embodiments that are illustrated in the accompanying drawings and detailed in the following description. It should be noted that the features illustrated in the drawings are not necessarily drawn to scale. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the present invention. The examples used herein are intended merely to facilitate an understanding of ways in which the invention may be practiced and to further enable those of skill in the art to practice the invention. Accordingly, the examples should not be construed as limiting the scope of the invention.

[0026] Every microelectronics wafer test facility deals with the problem of not having enough tools to handle the capacity on high volume products. The options to alleviate this issue are to purchase more testers, which can be very ex-

pensive, and have long lead times. The invention is a new process that optimizes retest by minimizing the number of chips retested, and maximizing the number of customer shippable parts. The invention increases productivity and reduces test cycle time, and also optimizes retest rates.

[0027] The invention performs the retest process to maximize the number of good chips at wafer test. A second pass test is required to recover any additional deliverable chips. The traditional methods retest all devices that fail the first pass test. One type of defect, Test Generated Yield Loss (TGYL), includes failures that may have been induced by test operation (i.e., for example, contact fail sort; operator setup problem, or bad probes).

[0028] The overall flow of the invention is shown in Figure 1. In item 100, the invention performs the initial testing, and retests all devices that failed the first pass testing results. The testing (first pass) and retesting (second pass) results are shown in spreadsheet form in Figure 2. These tables (spreadsheets) identify the lot and wafer that was tested (first two columns), the X and Y coordinates of the area of the wafer tested (next two columns) and the tested area's name (suffix column). The column entitled "sort" refers to

the type, or sort, of defect. Different types of defects identified during the testing process are given different numbers. The last column is a shorthand description of the defect type. Note that a "1" defect means that the area or device did not fail the test and is "good."

[0029] In item 102 in Figure 1, the invention creates the retest analysis dataset which is shown in Figure 3, and which combines the data from the first (Figure 2) and second pass (Figure 3) testing results into a single table. Note that separate columns are used to identify the different types of defects seen in the first and second passes. Items that passed the first testing are not retested as indicated by an asterisk in the second pass column.

[0030] In item 104, the invention runs a second pass status frequency analysis, which is shown in Figure 5. In Figure 5, the invention lists each type of defect by number (sort) and description and shows how many of these defects were found. The "bad" column counts the number of failures that were repeated during the retest, which presumably indicates a true defect. The number in the "Cat 2 Good" column represents the number of devices that had some defects, but were good enough to operate, although possibly with limited functionality or reduced speed/

performance. For example, many of the devices produced (chips or sections of chips) have redundant portions, or the devices need to have all areas formed correctly to operate at the highest speed (or provide the highest performance). However, some portions of the devices may have defects while the remainder of the device is defect free. Some customers will find these poorer performing or partially defective devices acceptable and may receive such devices at a reduced cost. Therefore, while the "category 2 good" devices underperform the completely defect free "good" devices, the category 2 good devices still have some demand (although a reduced demand). The "Good" column shows the number of devices that recovered (i.e., became good) in the 2^{nd} pass test. The "total" column is the total number of defects of that type that occurred during the first test. Therefore, as shown in Figure 5, for certain types of defects (e.g., sort 2, 3, etc.) a substantial number of devices retested as being good or category 2 good, which makes retesting for these types of defects worth the cost of retesting. To the contrary, other types of defects (e.g., sort 21, 22, 40, etc.) did not have as high a retest passing rate (or had a zero retest passing rate) and it may not be worth retesting devices with such types of

defects.

[0031] Next, in item 106, the invention obtains TGLY fail sorts from historical data, which are shown in Figure 6. The types of defects which are not normally associated with TGLY type failures are shown in Figure 7. The classifications show in the drawings are merely an example of one specific type of device and its associated failures and the invention is not limited to this example, but instead is applicable to any type of testing and commonly known defects that result from improper testing.

[0032] In item 108, the invention creates the sort recovery dataset, an example of which is shown in Figure 8. Figure 8 is similar to Figure 5, except Figure 8 includes the TGLY data. In item 110, the invention obtains product supply/demand information that is shown in Figure 9. A type of device having a "Good" rating is in high demand, while a device having a category 2 rating (Cat 2 Good) is determined to have a reduced demand. The criteria for determining whether a type of device will have a high or reduced demand will vary from device to device and from industry to industry, and, as discussed above, is based upon how many defects the device has.

[0033] In item 112, the invention creates the optimized retest ta-

ble that is shown in Figure 10 by adding the TGYL information to that shown in Figure 8. In addition, the optimized retest table includes a "retest sort" column which identifies whether each type of defect is approved for retesting upon initial test failure. The invention evaluates these statistics to determine which types of failures have retest passing rates above a predetermined threshold and labels those types of defects as being approved with a "Y" in the retest sort column. In addition TGYL type defects can also be approved for retest and given a "Y" in the retest sort column Regardless of their retest passing rates. If desired, only the higher demand type devices ("Good column") that have passing rates above a predetermined threshold are retested and the reduced demand devices ("Cat 2 Good column) are not retested.

[0034] As shown in Figure 11, the inventive system includes a tester 150 (e.g., probe-type tester), a database 160, and a processor 170. The database 160 includes an optimized retest table of the types of defects approved for retesting. Again, the types of defects approved for retesting is based upon previously acquired statistics of which types of failures have retest passing rates (after initially failing testing) above a predetermined threshold. In addition, defect

types that result from improper testing can be included in the types of defects approved for retesting. Once again, device types having reduced demand are sometimes not retested. The processor 170 directs the tester 150 to test groups of devices and retest only devices in the additional failing groups that have one of the types of defects approved for retesting, without testing device types that have reduced demand.

[0035] Stated differently, the system includes means for testing (the tester 150) an initial group of devices to produce an initial failing group of devices that failed the testing , wherein the devices in the initial failing group are identified by type of failure; means for retesting (the tester 150) the devices in the initial failing group to identify a retested passing group of devices that passed the retesting; means for analyzing (the processor 170) the devices in the retested passing group to produce statistics regarding the likelihood that a failing device will pass the retesting according to the type of failure; means for evaluating (the processor 170) the statistics to determine which types of failures have retest passing rates above a predetermined threshold to produce types of defects approved for retesting, and storing the same in the means for storing (the

database 160); means for testing (the tester 150) additional groups of devices to produce additional failing groups of devices that failed the testing of the additional groups; and means for retesting (the tester 150) only devices in the additional failing groups that have one of the types of defects approved for retesting.

[0036] A representative hardware environment for practicing the present invention is depicted in Fig. 12, which illustrates a typical hardware configuration of an information handling/computer system in accordance with the subject invention, having at least one processor or central processing unit (CPU) 11. CPUs 11 are interconnected via system bus 12 to random access memory (RAM)14, read-only memory (ROM) 16, an input/output (I/O) adapter 18 for connecting peripheral devices, such as disk units 21 and tape drives 40 to bus 12, user interface adapter 22 for connecting keyboard 24, mouse 26, speaker 28, microphone 32, and/or other user interface devices such as touch screen device (not shown) to bus 12, communication adapter 34 for connecting the information handling system to a data processing network, and display adapter 36 for connecting bus 12 to display device 38. A program storage device readable by the disk or tape units, is used

to load the instructions which operate the invention which is loaded also loaded onto the computer system.

[0037] Thus, with the invention, the data collected at wafer test is analyzed to optimize limits and rules on retest without sacrificing yield. It is important to retest failed devices to avoid discarding properly functioning devices. By not retesting all failed devices, substantial testing costs are saved. Reduction in the number of devices retested also reduces the number of touchdowns of the front end hardware.

[0038] The methodology of the invention begins by testing an initial group of devices (e.g., integrated circuit chips) to produce an initial failing group of devices that failed the testing. The devices in the initial failing group are identified by type of failure. Then, the invention retests the devices in the initial failing group to identify a retested passing group of devices that passed the retesting. Next, the invention analyzes the devices in the retested passing group which allows the invention to produce statistics regarding the likelihood that a failing device that failed the initial testing will pass the retesting according to the type of failure. Then, the invention evaluates these statistics to determine which types of failures have retest passing

rates above a predetermined threshold. From this the invention produces a database 160 comprising an optimized retest table listing the types of defects that are approved for retesting.

[0039] The invention can also identify types of devices having a predetermined reduced demand. For example, devices having a certain number of defects may no longer be in strong demand and it may not be worth the cost to retest these types of devices. Therefore, in one option, the invention can add a listing of item types having reduced demand to the database 160 to prevent such reduced demand items from being retested.

[0040] Further, some types of defects may be known to be related to improper testing. One contributor to test failures is bad or marginal probe contact due to reasons that include poor test setup and marginal/defective probe hardware. In order to eliminate improper testing errors, the invention can add types of defects associated with testing errors to the types of defects approved for retesting.

[0041] Using the information in the optimized retest table database 160, the invention then tests additional groups of devices to produce additional failing groups of devices. The invention only retests devices that have one of the

types of defects approved for retesting, and may not retest the types of devices for which there is the reduced demand. This process optimizes the retesting of the devices by only retesting for defects that have above a predetermined rate of retest passing.

[0042] In the example shown above, the invention reduced the chip retest rate by up to 80% when compared to retesting all failing devices. The invention can be performed without spending an excessive amount of money on new testers, and without impacting customer deliverables (i.e., no yield loss).

[0043] Some advantage of the invention vs. buying/leasing testers to alleviate test capacity issues can save in tester purchase/lease/maintenance costs. In one example, the invention takes less than one month to implement vs. 3-6 month lead time in obtaining new testers. The invention saves money in test time which alleviates test capacity issues. The invention improves delivery time to the customer by reducing test cycle time (fewer chips are retested). The retests are only performed on defect types that are proven to recover to customer deliverable devices. Thus, the invention increases the number of customer deliverable parts. The invention may recover parts

that were sorted as an atypical TGYL fail sort during the first pass test.

[0044] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.